synchronous memory (clocked) or asynchronous memory (non-clocked). Moreover, the dual read port microcode memory may be a synchronous burst or non-burst memory.

In yet another alternative embodiment, multiple address latches and multiple code word latches are used in a pipelined system. In this regard, code word data and address data are latched in a pipelined system having a plurality of clocked execution phases. A code word latch for storing code word data is opened during the Nth phase of a clock cycle to store the code word data read out from microcode memory to the code word latch. This code word latch is closed during the N+1th phase of a clock cycle, simultaneous with the opening of the address latch on the same phase. The address latch opens during the N+1th phase of a clock cycle to store the address data from the microcode controller for the subsequent phase of the clock cycle after the N+1th phase of a clock cycle. The foregoing sequence repeats as stated above, with alternating phases for the opening and closing of the address and code word latches for a plurality of phases of the clock cycle. For instance, the code word latch is open on odd phases clock cycles (i.e., 1, 3, 5, etc.) and is closed on even phase clock cycles (i.e., 2, 4, 6, etc.). Likewise, the address latch is open on even phase clock cycles and closed on odd phase clock cycles. A representative timing diagram showing a 4 phase clocking system is shown in Fig. 5.

It should be understood that all the improvements mentioned for decryption of data are likewise realized for encryption of data.

Fig. 6 provides timelines for a decryption operation that illustrate performance improvements contributed by the present invention. Section I is a timeline associated with the prior art, while Section II is a time line associated with the present invention. It should be appreciated that Section II also illustrates the effects provided by use of a dual ported key storage, as disclosed in related application serial no. 09675069, filed 9/28/2000, and assigned to the assignee of the present application. Dual ported key storage allows a key to be loaded into memory